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FABRICATION AND STUDYING THE CHARACTERISTICS OF ITO/CdTe/Si/Au THIN FILM SOLAR CELL

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ABSTRACT

The CdTe/Si solar cells have been fabricated on p-Si wafer by thermal evaporation method at different thicknesses of n-CdTe (100, 300, 500, and 700nm). The structural and electrical properties including x-ray diffraction, AFM analysis and I-V characteristics are studied and interpreted. For the back and front contacts, gold and indium tin oxide (ITO) are used respectively. Choosing gold as a good back contact is because of its suitable work function with respect to electron affinity and energy gap of silicon.

While ITO is chosen as a good front contact for its special properties of good conductivity and transparency. XRD patterns show a good crystallinity of CdTe films and AFM images show a good smoothness of the surface topography of these films. From Hall Effect measurements, we found that the mobilityof charge carriers is 820cm^2/V-s. From the I-V curves, we found that the quantum efficiency and fill factor have maximum values at the thickness of 500nm (η=3.61%, and FF=0.39).In general, the dark current of devices is very close to zero.

KEYWORDS: Solar Cell, CdTe, ITO, Quantum Efficiency

INTRODUCTION

Recently, more attention had been paid to theheterojunction devices research [1]. Good achievements ofheterojunctions are fully established in electronic devicessuch as solar cells, high quality lasers, and opticaldetectors [2]. Heterojunctions that consist of CdTe asone of the junction sides had been under research formany years.Efficient solar cell performance needs minimizing the forward recombination current and maximizing the light generated current. Losses can be minimized in thin film of high absorption and short diffusion length [3]. Some voltage dependent photocurrent collection losses in CdTe films were observed [4]. In the present work, I-V characteristics of Si–CdTe heterojunction are investigated as a function of thickness of CdTe layer. Other electrical properties are shown by Hall Effect measurements. Also, some structural characteristics are investigated through XRD patterns and AFM images.

EXPERIMENTAL

In this work CdTe (1:1) powder is used to deposit thin films on p-type siliconwafer (0.7mm)as substrate by thermal evaporation method using NANO 38 deposition systemsupplied by Kurt J. Lesker Company.The rate of deposition is set to be 0.05nm/sec for 100nm, 0.09nm/sec for 300nm, 0.13nm/sec for 500nm, and 0.17nm/sec for 700nm film thickness respectively so that the total time of the deposition process takes about one hour.

The thickness of layers is controlled by crystal quartz method.The substrate during the deposition process was not heated.The prepared samples are annealed in air for one hour at 300°C by plate heater. To prepare the silicon wafers for the deposition process, Shiraki cleaning is done then they are itched by HF for one minute to remove the oxide layer from them.For the back contact, 100nm gold layer is deposited on the back of silicon wafer by Sputtering method.As a front

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contact, 100nm layer of indium tin oxide (ITO) is deposited on the CdTe layer by Sputtering method. Figure1illustrates a schematic view of the solar cell layers.

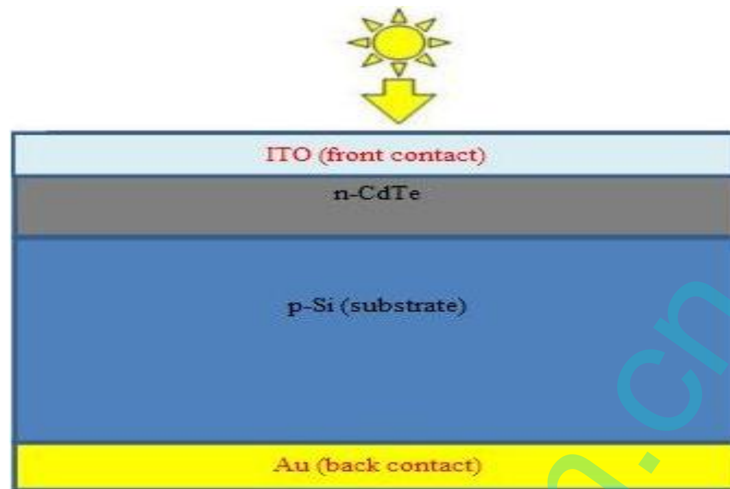

Figure 1: Schematic View of the Prepared Solar Cell

Samples are tested by XRD method using Ultima IV X-ray diffractometer supplied by Rigaku Co. For Hall Effect measurements, we used HMS-3000 VER 3.5 system supplied by ECOPIA. Also for AFM images, CSPM Imager Surface Roughness Analysissystem is used. Finally, I-V characteristics are measured by KEITHLEY computerized system after contact wires were soldered to each side of samples by indium alloy soldering.This type of soldering guarantees good contacts,as well as its low temperature keeps the structural properties of films unaffected.

RESULTS AND DISCUSSIONS

From XRD patterns of CdTe deposited layer, it is clear that the structure of films is polycrystalline with sharp peaks at different Bragg angles, 2θ=23.758, 39.311, 46.433, 56.820 and 62.351 degree corresponding to reflection surfaces (111), (220), (311), (400) and (331) respectively. And films have crystallized with a strong peak at (111) direction as shown in Fig.2, this means that this plane is suitable for crystal growth [5].

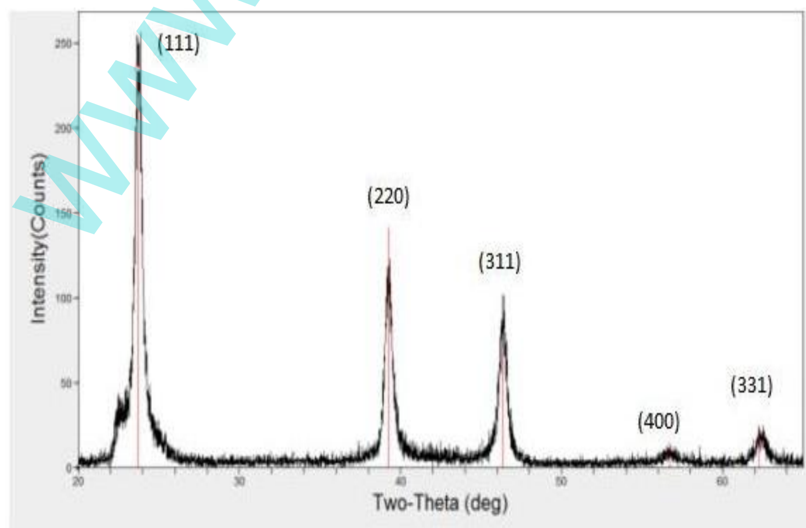

Figure 2: CdTe 100nm on Si, T_a=300°C

Figures 3 to 8 show two and three dimensional AFM images of the surface topography of CdTe film with 100nm thickness at room temperature.

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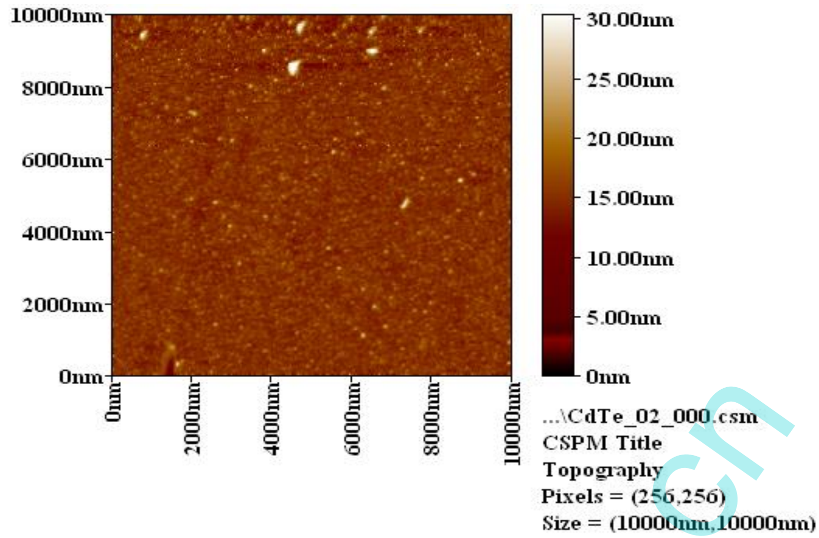

Figure 3: 2-D AFM Image of Surface Topography of 100nm CdTe Filmat RT

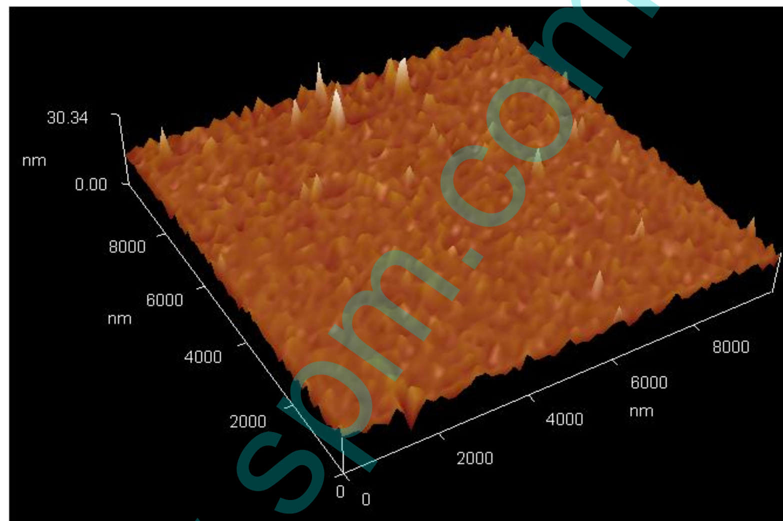

Figure 4: 3-D AFM Image of CdTe Film for the Same Snapshot of Figure 3

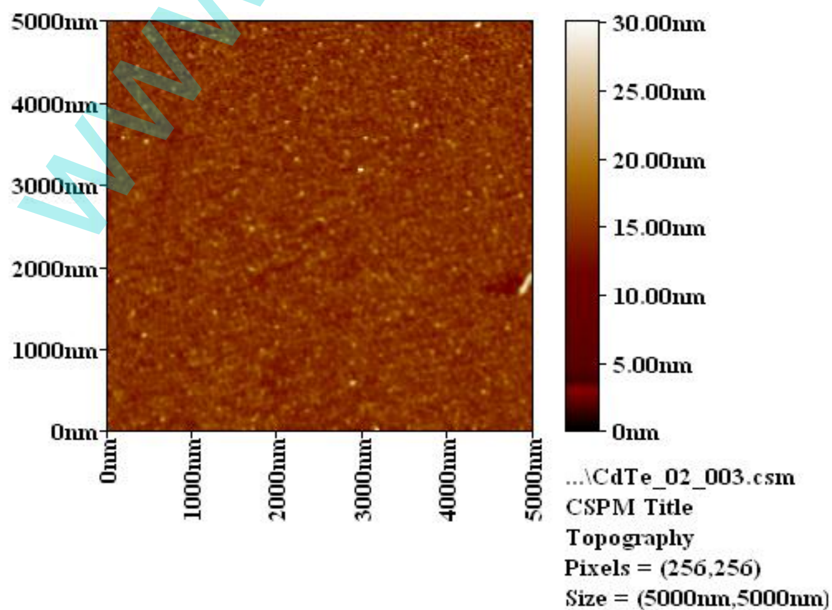

Figure 5: Closer View of Figure 3

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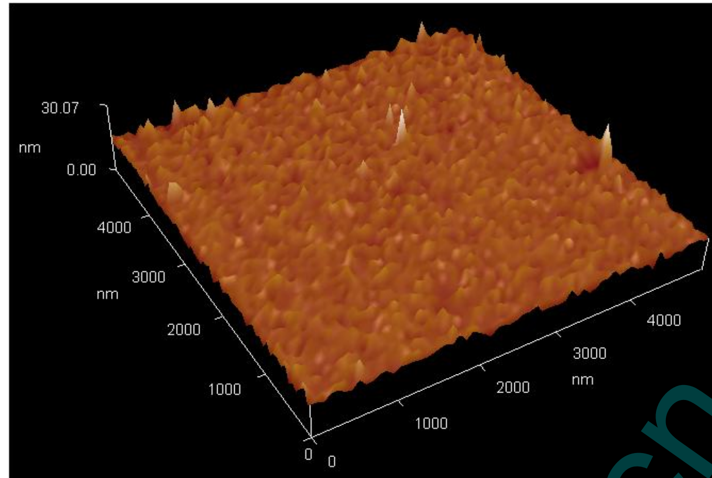

Figure 6: 3-D View of Figure 5

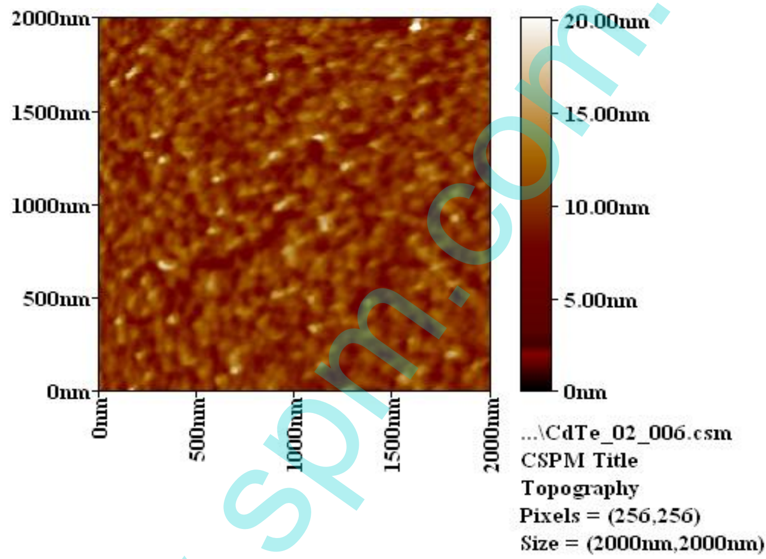

Figure 7: Closer View of Figure 5

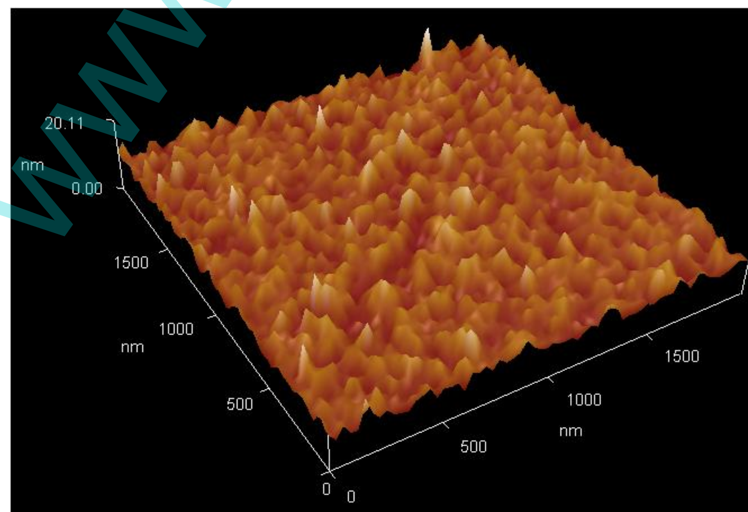

Figure 8: 3-D View of Figure 7

In these images, S_a (Surface Roughness Average) is 0.615nm which shows very good smoothness of the surfacetopography and that means our filmsare deposited very well. Table (1) summarizes surface topography parameters for all CdTe layer thicknesses.

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Table 1: Surface Topography Parameters for Deposited CdTe Thicknesses

Thickness (nm)	100	300	500	700
Surface Roughness Average (nm)	0.615	0.706	1.17	1.58
Root Mean Square (nm)	0.839	0.915	1.52	2.08
Ten Point Height (nm)	7.21	7.98	13.1	13.9

The results of Hall Effect measurements are summarized in table (2).Obviously, the negative sign of Hall coefficient indicates that the charge carriers are electrons as predicted for n-type semiconductor. The obtained value of mobility, 820cm^2/V-s, is interestingly higher than reported values [6, 7];while for other parameters, such aselectron concentrations (bulk and sheet)and resistivity, the values are comparable.It could be concluded that using Si substrate for depositing CdTe on it considerably increases the mobility of charge carriers.

Table 2: Hall Effect Measurements at Room Temperature for 100nm CdTe/Si Film Averaged over 1000 Times

Parameter	Value
Bulk Concentration (1/cm^3)	-6.577E+10
Sheet Concentration (1/cm^2)	-6.577E+5
Mobility (cm^2/V-s)	8.202E+2
Conductivity (1/Ωcm)	8.642E-6
Resistivity (Ω cm)	1.157E+5
Average Hall Coefficient (m^2/C)	-9.492E+7
Magneto-resistance (Ω)	2.096E+9

The quantum efficiency, η, and the fill factor, FF, are calculated from I-V characteristics diagrams. Fig.9is for dark and fig.10 for light current when the thickness of the CdTe layer is 500nm which has the maximum values of η and FF.The dark current in the reverse bias is very close to zero which could be considered as an ideal case for diode characteristics.

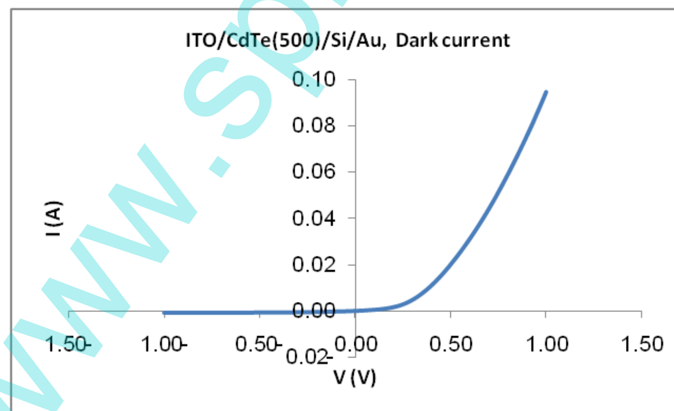

Figure 9: I-V Curve of Dark Current for ITO/CdTe/Si/Au Device in which the Thickness of CdTe is 500nm

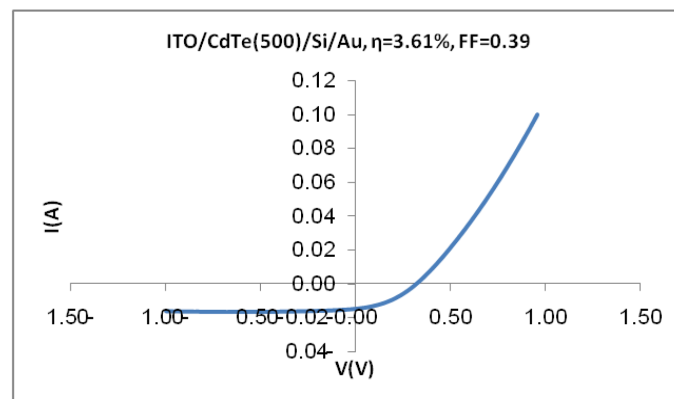

Figure 10: I-V Curve of Light Current for the Same Device

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To calculate the quantum efficiency,we use the relationship (1)

$\eta = P_{out}/P_{in}$ ………… (1)

WhereP_{in}=0.06 W/$cm^2$is the power per area forthe halogen lamp measured by power meter.

$P_{out} = P_{max}/A$ ………… (2)

Here A is the effective area of the device in units of cm^2 and P_{max} is the maximum absolute value of the product of 'I' and 'V' data in the fourth region of coordinates. Also we use

$FF = P_{max}/ (V_{oc} * I_{sc})$ ……… (3)

Where V_{oc} is the open circuit voltage and I_{sc} is the short circuit current. All I-V results of other thicknesses also, are summarized in table (3).

Table 3: Values of η and FF for Fabricated Solar Cells with Different Thicknesses of CdTe Films

Thickness of CdTe layer (nm)	100	300	500	700
Quantum efficiency, (η %)	0.7	0.94	3.61	0.33
Fill factor, FF	0.28	0.29	0.39	0.27

From table (3) we can conclude that both η and FF increase with increasing the thickness of CdTe layer up to maximum values 3.61% and 0.39 respectively, and then decrease. This behavior is due to penetration depth of light into CdTe layer. This depth changes proportional to the wave length of illuminated light [8, 9]. Higher energy light is of a shorter wavelength and has a shorter absorption depth than lower energy light, which is not as readily absorbed, and has a greater absorption depth.So, for some thickness of CdTe film, the absorbed light reaches its maximum amount through the interface region and consequently into the depletion layer and creates a maximum amount of photocurrent,and after that specific thickness, the photocurrent decreases. Choosing gold for back contact is because of its suitable work function with respect to electron affinityandenergy gapofsilicon.The electron affinity of p-Si is 4.05eV and its energy gap at 300K is 1.12eV [10]. The work function of a metal to be a good ohmic contact for some material must be equal or higher than the sum of electron affinityandenergy gap of that material. The work function of gold is in the range of 5.1 and 5.47eV which could be ideal for this goal [11]. Table (4) shows work function for some metals.

Table 4: Work Function Values for Some Metals (Source: Wikipedia, The Free Encyclopedia)

Metal	Ag	Al	Au	Cu	Fe
Work function	4.52-4.74	4.06-4.26	5.1-5.47	4.53-5.1	4.67-4.81

On the other hand, for n-CdTe the ohmic contact on the junction is not difficult to achieve [12]. Although the sum of electron affinity and energy gap of CdTe is 5.73eV [13] which is greater than the work function of ITO, 5.53eV [14],but for n-type semiconductors the case is different.For an n-type semiconductor an ohmic contact means that the work functionof the metal must be closer or smaller than the electron affinity of the semiconductor [11]. The most important property of ITO to be chosen as front contact is its transparency.So, in contrary with other conductors, it allows light to pass through it without any problem.

CONCLUSIONS

By varying the thickness of CdTe film, the quantum efficiency and fill factor increase, reach their maximum values at the thickness of 500nm, and then decrease. Probably this behavior is due to penetration depth of light into CdTe layer. Using p-type silicon wafer as a substrate and in the same time as a p-side of the junction considerably increases the

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mobility of charge carriers. XRD patterns and AFM images show that the deposited CdTe layer on Si wafer has a good situation. Gold at back and ITO at front are suitable contacts for the CdTe/Si heterojunction.

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